

## Standard 8K x 8 SRAM

### Features

- 8192 x 8 bit static CMOS RAM
- 70 and 100 ns Access Times
- Common data inputs and outputs
- Three-state outputs
- Typ. operating supply current
  - 70 ns: 45 mA
  - 100 ns: 37 mA
- Data retention current at 3 V: < 10  $\mu$ A (standard)
- Standby current standard < 30  $\mu$ A
- Standby current low power (L) < 10  $\mu$ A
- Standby current very low power (LL) < 1  $\mu$ A
- Standby current for LL-version at 25  $^{\circ}$ C and 5 V: typ. 50 nA
- TTL/CMOS-compatible
- Automatic reduction of power dissipation in long Read or Write cycles
- Power supply voltage 5 V
- Operating temperature ranges:
  - 0 to 70  $^{\circ}$ C
  - 25 to 85  $^{\circ}$ C
  - 40 to 85  $^{\circ}$ C
- Quality assessment according to CECC 90000, CECC 90100 and CECC 90111

- ESD protection > 2000 V (MIL STD 883C M3015.7)
- Latch-up immunity > 100 mA
- Packages: PDIP28 (600 mil)  
SOP28 (300 mil)  
SOP28 (330 mil)

### Description

The U6264A is a static RAM manufactured using a CMOS process technology with the following operating modes:

- Read            - Standby
- Write         - Data Retention

The memory array is based on a 6-transistor cell.

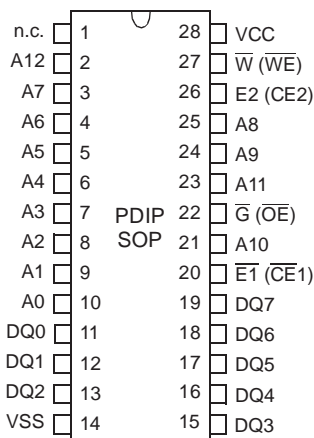
The circuit is activated by the rising edge of E2 (at  $\overline{E1} = L$ ), or the falling edge of  $\overline{E1}$  (at E2 = H). The address and control inputs open simultaneously. According to the information of  $\overline{W}$  and  $\overline{G}$ , the data inputs, or outputs, are active. During the active state ( $\overline{E1} = L$  and E2 = H), each address change leads to a new Read or Write cycle. In a Read cycle, the data outputs are activated by the falling edge of  $\overline{G}$ , afterwards the data word read will be available at the outputs

DQ0 - DQ7. After the address change, the data outputs go High-Z until the new read information is available. The data outputs have no preferred state. If the memory is driven by CMOS levels in the active state, and if there is no change of the address, data input and control signals  $\overline{W}$  or  $\overline{G}$ , the operating current (at  $I_O = 0$  mA) drops to the value of the operating current in the Standby mode. The Read cycle is finished by the falling edge of E2 or  $\overline{W}$ , or by the rising edge of E1, respectively.

Data retention is guaranteed down to 2 V. With the exception of E2, all inputs consist of NOR gates, so that no pull-up/pull-down resistors are required. This gate circuit allows to achieve low power standby requirements by activation with TTL-levels too.

If the circuit is inactivated by E2 = L, the standby current (TTL) drops to 150  $\mu$ A typ.

### Pin Configuration



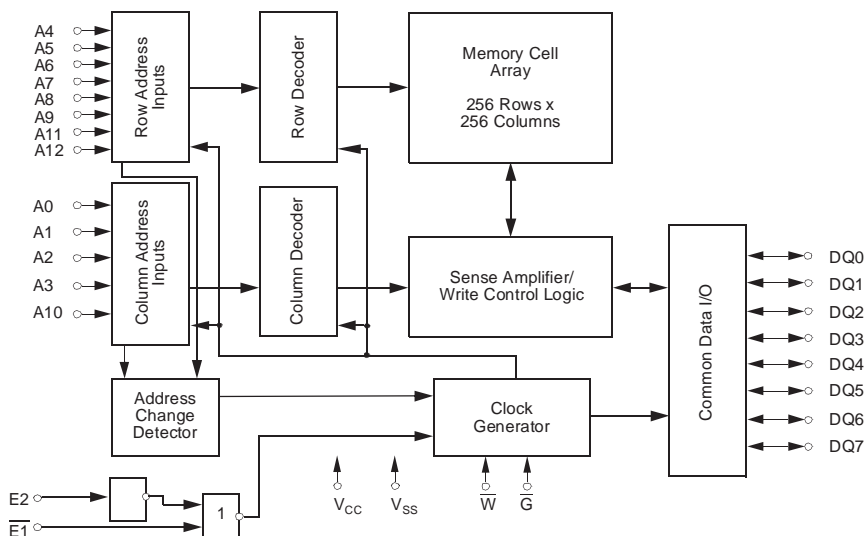
Top View

### Pin Description

| Signal Name    | Signal Description   |
|----------------|----------------------|
| A0 - A12       | Address Inputs       |
| DQ0 - DQ7      | Data In/Out          |
| E1             | Chip Enable 1        |
| E2             | Chip Enable 2        |
| $\overline{G}$ | Output Enable        |
| $\overline{W}$ | Write Enable         |
| VCC            | Power Supply Voltage |
| VSS            | Ground               |
| n.c.           | not connected        |

# U6264A

## Block Diagram



## Truth Table

| Operating Mode       | $\bar{E}_1$ | $E_2$ | $\bar{W}$ | $\bar{G}$ | DQ0 - DQ7          |
|----------------------|-------------|-------|-----------|-----------|--------------------|
| Standby/not selected | *           | L     | *         | *         | High-Z             |
|                      | H           | *     | *         | *         | High-Z             |
| Internal Read        | L           | H     | H         | H         | High-Z             |
| Read                 | L           | H     | H         | L         | Data Outputs Low-Z |
| Write                | L           | H     | L         | *         | Data Inputs High-Z |

\* H or L

## Characteristics

All voltages are referenced to  $V_{SS} = 0$  V (ground).

All characteristics are valid in the power supply voltage range and in the operating temperature range specified.

Dynamic measurements are based on a rise and fall time of  $\leq 5$  ns, measured between 10% and 90% of  $V_i$ , as well as input levels of  $V_{iL} = 0$  V and  $V_{iH} = 3$  V. The timing reference level of all input and output signals is 1.5 V, with the exception of the  $t_{dis}$ -times, in which cases transition is measured  $\pm 200$  mV from steady-state voltage.

| Maximum Ratings       | Symbol    | Min. | Max.           | Unit               |
|-----------------------|-----------|------|----------------|--------------------|
| Power Supply Voltage  | $V_{CC}$  | -0.3 | 7              | V                  |
| Input Voltage         | $V_i$     | -0.3 | $V_{CC} + 0.5$ | V                  |
| Output Voltage        | $V_o$     | -0.3 | $V_{CC} + 0.5$ | V                  |
| Power Dissipation     | $P_D$     | -    | 1              | W                  |
| Operating Temperature | C-Type    | 0    | 70             | $^{\circ}\text{C}$ |
|                       | G-Type    | -25  | 85             | $^{\circ}\text{C}$ |
|                       | K-Type    | -40  | 85             | $^{\circ}\text{C}$ |
| Storage Temperature   | $T_{stg}$ | -55  | 125            | $^{\circ}\text{C}$ |

| Recommended Operating Conditions | Symbol       | Conditions | Min. | Max.           | Unit |
|----------------------------------|--------------|------------|------|----------------|------|
| Power Supply Voltage             | $V_{CC}$     |            | 4.5  | 5.5            | V    |
| Data Retention Voltage           | $V_{CC(DR)}$ |            | 2.0  |                | V    |
| Input Low Voltage*               | $V_{IL}$     |            | -0.3 | 0.8            | V    |
| Input High Voltage               | $V_{IH}$     |            | 2.2  | $V_{CC} + 0.3$ | V    |

\* -2 V at Pulse Width 10 ns

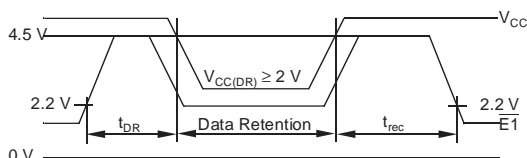
| Electrical Characteristics                 | Symbol        | Conditions   | Min. | Max.     | Unit          |
|--|---------------|--|------|----------|---------------|
| Supply Current - Operating Mode            | $I_{CC(OP)}$  | $V_{CC} = 5.5\text{ V}$<br>$V_{IL} = 0.8\text{ V}$<br>$V_{IH} = 2.2\text{ V}$                            |      |          |               |
| Standard                                   |               | $t_{cW} = 70\text{ ns}$<br>$t_{cW} = 100\text{ ns}$  |      | 70<br>60 | mA<br>mA      |
| Low Power (L)                              |               | $t_{cW} = 70\text{ ns}$<br>$t_{cW} = 100\text{ ns}$  |      | 70<br>60 | mA<br>mA      |
| Very Low Power (LL)                        |               | $t_{cW} = 70\text{ ns}$<br>$t_{cW} = 100\text{ ns}$  |      | 55<br>45 | mA<br>mA      |
| Supply Current - Standby Mode (CMOS level) | $I_{CC(SB)}$  | $V_{CC} = 5.5\text{ V}$<br>$V_{E1} = V_{E2} = V_{CC} - 0.2\text{ V}$<br>or $V_{E2} = 0.2\text{ V}$       |      |          |               |
| Standard                                   |               |  |      | 30       | $\mu\text{A}$ |
| Low Power (L)                              |               |  |      | 10       | $\mu\text{A}$ |
| Very Low Power (LL)                        |               |  |      | 1        | $\mu\text{A}$ |
| Supply Current - Standby Mode (TTL level)  | $I_{CC(SB)1}$ | $V_{CC} = 5.5\text{ V}$<br>$V_{E1} = V_{E2} = 2.2\text{ V}$<br>or $V_{E2} = 0.2\text{ V}$                |      |          |               |
| Standard                                   |               |  |      | 5        | mA            |
| Low Power (L)                              |               |  |      | 5        | mA            |
| Very Low Power (LL)                        |               |  |      | 3        | mA            |
| Supply Current - Data Retention Mode       | $I_{CC(DR)}$  | $V_{CC(DR)} = 3\text{ V}$<br>$V_{E1} = V_{E2} = V_{CC(DR)} - 0.2\text{ V}$<br>or $V_{E2} = 0.2\text{ V}$ |      |          |               |
| Standard                                   |               |  |      | 10       | $\mu\text{A}$ |
| Low Power (L)                              |               |  |      | 10       | $\mu\text{A}$ |
| Very Low Power (LL)                        |               |  |      | 1        | $\mu\text{A}$ |

# U6264A

| Electrical Characteristics                            | Symbol    | Conditions   | Min. | Max. | Unit          |
|---|-----------|--|------|------|---------------|
| Output High Voltage                                   | $V_{OH}$  | $V_{CC} = 4.5\text{ V}$<br>$I_{OH} = -1.0\text{ mA}$ | 2.4  |      | V             |
| Output Low Voltage                                    | $V_{OL}$  | $V_{CC} = 4.5\text{ V}$<br>$I_{OL} = 3.2\text{ mA}$  |      | 0.4  | V             |
| Input Leakage Current<br>Standard &<br>Low Power (L)  |           |  |      |      |               |
| High  | $I_{IH}$  | $V_{CC} = 5.5\text{ V}$<br>$V_{IH} = 5.5\text{ V}$   |      | 2    | $\mu\text{A}$ |
| Low   | $I_{IL}$  | $V_{CC} = 5.5\text{ V}$<br>$V_{IL} = 0\text{ V}$     | -2   |      | $\mu\text{A}$ |
| Very Low Power (LL)                                   |           |  |      |      |               |
| High  | $I_{IH}$  | $V_{CC} = 5.5\text{ V}$<br>$V_{IH} = 5.5\text{ V}$   |      | 1    | $\mu\text{A}$ |
| Low   | $I_{IL}$  | $V_{CC} = 5.5\text{ V}$<br>$V_{IL} = 0\text{ V}$     | -1   |      | $\mu\text{A}$ |
| Output High Current                                   | $I_{OH}$  | $V_{CC} = 4.5\text{ V}$<br>$V_{OH} = 2.4\text{ V}$   |      | -1   | mA            |
| Output Low Current                                    | $I_{OL}$  | $V_{CC} = 4.5\text{ V}$<br>$V_{OL} = 0.4\text{ V}$   | 3.2  |      | mA            |
| Output Leakage Current<br>Standard &<br>Low Power (L) |           |  |      |      |               |
| High at Three-State Outputs                           | $I_{OHZ}$ | $V_{CC} = 5.5\text{ V}$<br>$V_{OH} = 5.5\text{ V}$   |      | 2    | $\mu\text{A}$ |
| Low at Three-State Outputs                            | $I_{OLZ}$ | $V_{CC} = 5.5\text{ V}$<br>$V_{OL} = 0\text{ V}$     | -2   |      | $\mu\text{A}$ |
| Very Low Power (LL)                                   |           |  |      |      |               |
| High at Three-State Outputs                           | $I_{OHZ}$ | $V_{CC} = 5.5\text{ V}$<br>$V_{OH} = 5.5\text{ V}$   |      | 1    | $\mu\text{A}$ |
| Low at Three-State Outputs                            | $I_{OLZ}$ | $V_{CC} = 5.5\text{ V}$<br>$V_{OL} = 0\text{ V}$     | -1   | -    | $\mu\text{A}$ |

| Switching Characteristics                          | Symbol     |              | Min. |     | Max. |     | Unit |
|--|------------|--------------|------|-----|------|-----|------|
|  | Alt.       | IEC          | 07   | 10  | 07   | 10  |      |
| Time to Output in Low-Z                            | $t_{LZ}$   | $t_{t(QX)}$  | 5    | 5   | 10   | 10  | ns   |
| Cycle Time   |            |              |      |     |      |     |      |
| Write Cycle Time                                   | $t_{WC}$   | $t_{cW}$     | 70   | 100 |      |     | ns   |
| Read Cycle Time                                    | $t_{RC}$   | $t_{cR}$     | 70   | 100 |      |     | ns   |
| Access Time  |            |              |      |     |      |     |      |
| $\overline{E1}$ LOW or E2 HIGH to Data Valid       | $t_{ACE}$  | $t_{a(E)}$   | -    | -   | 70   | 100 | ns   |
| $\overline{G}$ LOW to Data Valid                   | $t_{OE}$   | $t_{a(G)}$   | -    | -   | 40   | 50  | ns   |
| Address to Data Valid                              | $t_{AA}$   | $t_{a(A)}$   | -    | -   | 70   | 100 | ns   |
| Pulse Widths                                       |            |              |      |     |      |     |      |
| Write Pulse Width                                  | $t_{WP}$   | $t_{w(W)}$   | 50   | 70  |      |     | ns   |
| Chip Enable to End of Write                        | $t_{CW}$   | $t_{w(E)}$   | 65   | 90  |      |     | ns   |
| Setup Times  |            |              |      |     |      |     |      |
| Address Setup Time                                 | $t_{AS}$   | $t_{su(A)}$  | 0    | 0   |      |     | ns   |
| Chip Enable to End of Write                        | $t_{CW}$   | $t_{su(E)}$  | 65   | 90  |      |     | ns   |
| Write Pulse Width                                  | $t_{WP}$   | $t_{su(W)}$  | 50   | 70  |      |     | ns   |
| Data Setup Time                                    | $t_{DS}$   | $t_{su(D)}$  | 35   | 40  |      |     | ns   |
| Data Hold Time                                     |            |              |      |     |      |     |      |
| Address Hold from End of Write                     | $t_{DH}$   | $t_{h(D)}$   | 0    | 0   |      |     | ns   |
|  | $t_{AH}$   | $t_{h(A)}$   | 0    | 0   |      |     | ns   |
| Output Hold Time from Address Change               | $t_{OH}$   | $t_{v(A)}$   | 5    | 5   |      |     | ns   |
| $\overline{E1}$ HIGH or E2 LOW to Output in High-Z | $t_{HZCE}$ | $t_{dis(E)}$ | 0    | 0   | 25   | 35  | ns   |
| $\overline{W}$ LOW to Output in High-Z             | $t_{HZWE}$ | $t_{dis(W)}$ | 0    | 0   | 30   | 35  | ns   |
| $\overline{G}$ HIGH to Output in High-Z            | $t_{HZOE}$ | $t_{dis(G)}$ | 0    | 0   | 25   | 35  | ns   |

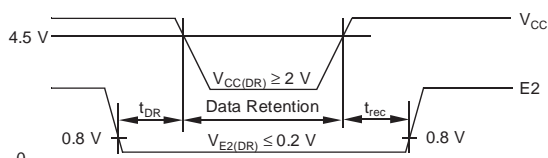
### Data Retention Mode $\overline{E1}$ -Controlled



$$V_{E2(DR)} \geq V_{CC(DR)} - 0.2 \text{ V or } V_{E2(DR)} \leq 0.2 \text{ V}$$

$$V_{CC(DR)} - 0.2 \text{ V} \leq V_{E1(DR)} \leq V_{CC(DR)} + 0.3 \text{ V}$$

### Data Retention Mode E2-Controlled



Chip Deselect to Data Retention Time

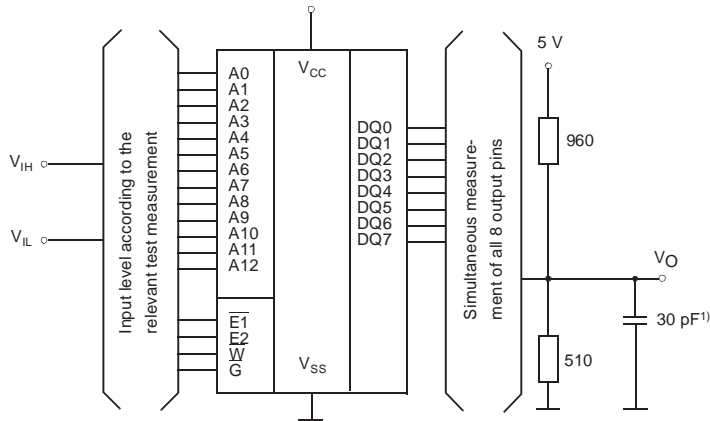
$t_{DR}$ : min 0 ns

Operating Recovery Time

$t_{rec}$ : min  $t_{cR}$

# U6264A

## Test Configuration for Functional Check



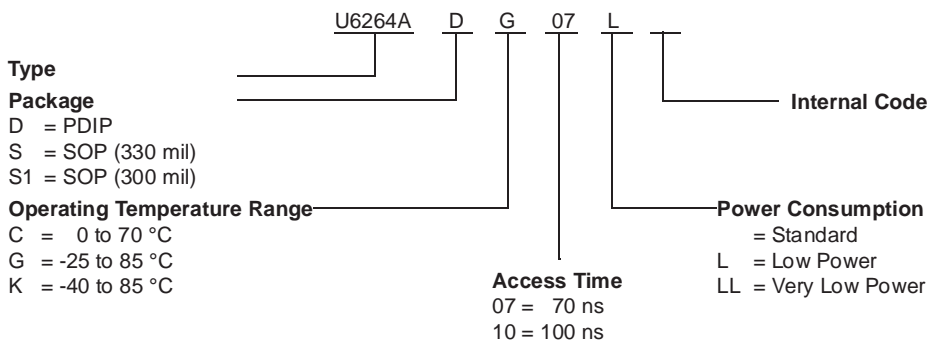
1) In measurement of  $t_{dis(E)}$ ,  $t_{dis(W)}$ ,  $t_{dis(G)}$  the capacitance is 5 pF.

| Capacitance        | Conditions                                     | Symbol | Min. | Max. | Unit |
|--------------------|--|--------|------|------|------|
| Input Capacitance  | $V_{CC} = 5.0\text{ V}$<br>$V_I = V_{SS}$      | $C_I$  |      | 8    | pF   |
| Output Capacitance | $f = 1\text{ MHz}$<br>$T_a = 25^\circ\text{C}$ | $C_O$  |      | 10   | pF   |

All pins not under test must be connected with ground by capacitors.

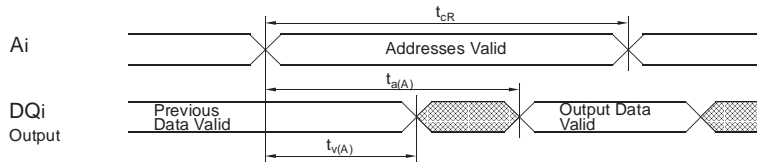
## IC Code Numbers

Example

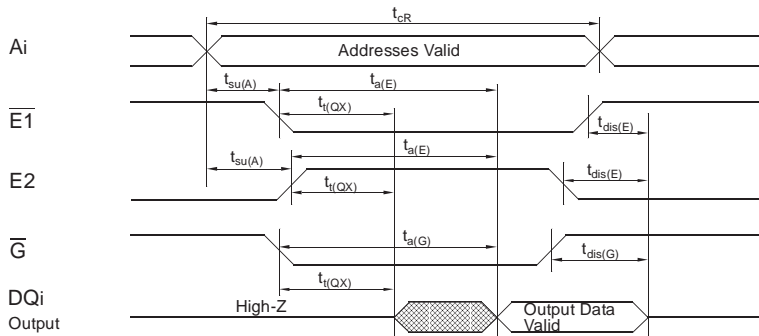


The date of manufacture is given by the last 4 digits of the mark, the first 2 digits indicating the year, and the last 2 digits the calendar week.

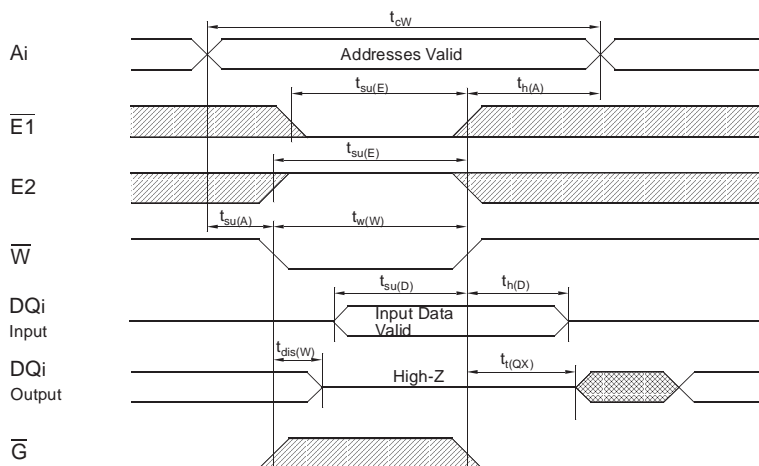
Read Cycle 1 (during Read cycle:  $\overline{E1} = \overline{G} = V_{IL}$ ,  $E2 = \overline{W} = V_{IH}$ )



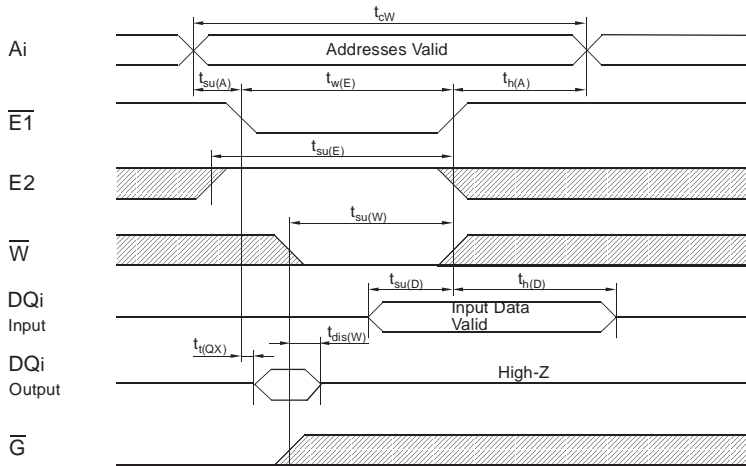
Read Cycle 2 (during Read cycle:  $\overline{W} = V_{IH}$ )



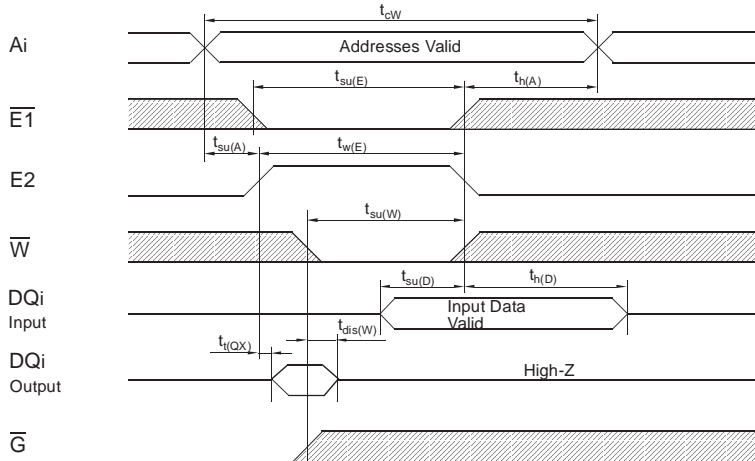
Write Cycle 1 ( $\overline{W}$ -controlled)



## Write Cycle 2 ( $\overline{E1}$ -controlled)



## Write Cycle 3 (E2-controlled)



undefined



L- or H-level







## **Memory Products 1998**

### **Standard 8K x 8 SRAM U6264A**

#### **LIFE SUPPORT POLICY**

ZMD products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the ZMD product could create a situation where personal injury or death may occur. Components used in life-support devices or systems must be expressly authorized by ZMD for such purpose.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

#### **Zentrum Mikroelektronik Dresden GmbH**

Grenzstraße 28 • D-01109 Dresden • P. O. B. 80 01 34 • D-01101 Dresden • Germany  
Phone: +49 351 88 22-3 06 • Fax: +49 351 88 22-3 37 • Email: sales@zmd.de  
Internet Web Site: <http://www.zmd.de>